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EXAMINER	
KIELIN, ERIK J	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 06/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,069	RAMANATH ET AL.	
	Examiner	Art Unit	
	Erik Kielin	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-11 and 13-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-11 and 13-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 May 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 23 May 2003 has been entered.

Information Disclosure Statement

2. Examiner acknowledges Applicant's remarks in response to the objection to the IDS that an IDS had been filed about one month prior to the mailing of the first Office action on the merits. This IDS was not, however, matched with the application until after mailing of the action and Examiner was clearly unaware that such IDS existed. Examiner apologizes on behalf of the Office for any inconvenience.

Nonetheless, the information disclosure statement filed 18 July 2002 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because some of the references have not been provided with dates in accordance with 37 CFR 1.98(b)(5). Also the MPEP 609 states,

> "Each publication must be identified by publisher, author (if any), title, relevant pages of the publication, and **date** and place of publication. The date of publication supplied must include at least the **month and year** of publication, except that **the year of publication (without the month) will be accepted if the applicant points out in the information disclosure statement that the year of publication is sufficiently earlier than the**

effective U.S. filing date and any foreign priority date so that the particular month of publication is not in issue." (Emphasis added.)

The IDS has been placed in the application file, but only the references initialed by Examiner have been considered. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

This is repeated from the Office action filed 25 February 2003.

Drawings

3. The corrected or substitute drawings were received on 23 May 2003. These drawings are acceptable.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims **6**-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,079,600 (**Schnur** et al.) in view of ASM Handbook Vol. 5, Surface Engineering, ASM International: Matierals Park, Ohio, 1994, pp. 315-318, and the basic textbook by **Porterfield**,

Inorganic Chemistry, A Unified Approach, Addison-Wesley: Reading, Massachusetts, 1984, pp. 487-488.

Regarding claim 6, **Schnur** discloses a semiconductor device comprising,

(a) a substrate (Fig. 1A);

(b) a diffusion barrier (Fig. 1A, called "thin film"), wherein the diffusion barrier comprises a self-assembled monolayer, SAM, (col. 10, lines 42-47) including a plurality of molecules, each molecule having an aromatic group at the terminus of the molecule. (For example, EXAMPLE 28 at col. 21, discloses a SAM formed from trichloro-(4-pyridyl)-ethyl-silane which forms the equivalent SAM barrier layer as shown in structure entitled "1" on p. 7 of the instant specification. The pyridyl is an aromatic group.

(c) a metal layer (called "catalyst" and "metal layer") on the diffusion barrier.

In pertinent part, **Schnur** states in col. 20,

> "EXAMPLE 24
> "Fabrication of MOS capacitor test structures.
> "An n-type silicon wafer with a 100 nm thick thermal oxide layer was cleaned and treated with UTF3 as in example 14. The film was patterned using a mask with standard capacitor test structures and irradiated for 28 minutes with an Hg/Ar lamp. The wafer was metallized with the standard copper plating procedures, used in Example 5, yielding metal squares 800 microns on a side (area=$6x10^{-3}$ cm^2). The metal/thermal oxide/n-type silicon (MOS) capacitors were then characterized by probing the metal pads and the back of the wafer with a Micromanipulator automatic C-V measuring system. The capacitance was found to be 26 pF/cm^2 with minimal (10 mV) hysteresis and remained stable at room temperature for at over 3 weeks, indicating that device degradation due to masked metal contamination (**diffusion of copper into the thermal oxide) was not a problem**. (Emphasis added.)

Accordingly, it is seen to be inherent that the SAM of **Schnur** is a diffusion barrier because **Schnur** states that "diffusion of copper into the thermal oxide" does not occur.

(See also section entitled, "Summary of the Invention") the sections entitled "EXAMPLE 1" col. 11, lines 24-58 wherein the barrier layer is formed from "octenyldimethylchlorosilane" covalently bonded to the substrate. See also "EXAMPLE 3" and "EXAMPLE 5.")

Schnur does not teach that the catalyst is copper, thereby having the limitation that "for each molecule of the plurality of molecules, the copper in the metal layer is in direct contact with the aromatic group of the molecule."

ASM Handbook teaches that copper may be used as a catalyst for electroless plating of copper (pp. 315-318 --especially p. 318 sections entitled, "Catalyzation" and "Copper catalyst"). The basic textbook of **Porterfield** ensures that copper forms metal complexes with pyridine groups, such as the pyridine group used in **Schnur** as the polar end-group of each molecule in the SAM barrier layer.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use copper as the metal catalyst in **Schnur** as taught in the **ASM Handbook** because **Schnur** is not limited to Pd/Sn catalysts, as at least claim 1 of **Schnur** makes clear, and because copper is a known catalyst for electroless copper plating, as used in **Schnur**, as taught by the **ASM Handbook**. In this regard, it has been held that the selection of a known material based upon its suitability for an intended purpose is obvious.

Schnur only requires that the catalyst bond to polar end group of the molecule which is the pyridyl end group of "Example 28" in **Schnur**. **Porterfield** ensures that such bonding occurs, such the one of ordinary skill has a reasonable expectation of success for using copper instead of Pd/Sn, as the catalyst in **Schnur**. Accordingly, using copper as the catalyst gives the

limitation, that "for each molecule of the plurality of molecules, the copper in the metal layer is in direct contact with the aromatic group of the molecule."

Regarding claim 7, as noted above, Example 24 in **Schnur** states that the substrate is a silicon wafer with silicon oxide formed thereon.

Regarding claim 8, **Schnur** discloses the linear carbon chain of trichloro-(4-pyridyl)-ethyl-silane is the ethyl group, which has at least 2 carbon atoms.

Regarding claim 10, it is held absent evidence to the contrary, that the diffusion barrier of **Schnur** is capable of preventing the diffusion of metal atoms from the metal layer into the substrate when the semiconductor device is exposed to thermal annealing at 200 °C or an electric field of 2 MV/cm at 200 °C in flowing N_2. Basis for this reasoning is that Applicant is using the exact same SAM, as is **Schnur** to form the barrier layer. **Schnur** also points out in Example 24 that copper diffusion does not occur even under the stress of an electric field. See *In re Swinhart*, 169 USPQ 226,229 (CCPA 1971) (where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that subject matter shown to be in the prior art does not possess the characteristics relied on) and *In re Fitzgerald*, 205 USPQ 594 (CCPA 1980) (the burden of proof can be shifted to the applicant to show that subject matter of the prior art does not possess the characteristic relied on whether the rejection is based on inherency under 35 USC 102 or obviousness under 35 USC 103). Note that as long as there is evidence of record establishing inherency, failure of those skilled in the art to contemporaneously recognize an inherent property, function or ingredient of a prior art reference does not preclude a finding of

anticipation. *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1349, 51 USPQ2d 1943, 1948 (Fed. Cir. 1999) (Two prior art references disclosed blasting compositions containing water-in-oil emulsions with identical ingredients to those claimed, in overlapping ranges with the claimed composition. The only element of the claims arguably not present in the prior art compositions was "sufficient aeration . . . entrapped to enhance sensitivity to a substantial degree." The Federal Circuit found that the emulsions described in both references would inevitably and inherently have "sufficient aeration" to sensitize the compound in the claimed ranges based on the evidence of record (including test data and expert testimony). This finding of inherency was not defeated by the fact that one of the references taught away from air entrapment or purposeful aeration.). See also *In re King*, 801 F.2d 1324, 1327, 231 USPQ 136, 139 (Fed. Cir. 1986); *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 782, 227 USPQ 773, 778 (Fed. Cir. 1985).

Regarding claim 12, the metal layer is in direct contact with the terminal groups of the molecules in self-assembled monolayer (Fig. 1A). Note that the "catalyst" is a metal and therefore forms part of the "metal layer."

6. Claims 9, 11, and **13**-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Schnur** in view of the **ASM Handbook** and **Porterfield**, as applied to claims 6-8 and 10 above, and further in view of **Wolf**, et al. Silicon Processing for the VLSI Era, Vol. 1-Process Technology, 2nd ed., Lattice Press: Sunset Beach CA, 2000, pp. 438, 782-783.

Regarding claims 9 and 13, **Schnur** discloses each of the claimed features, as explained above, but does not indicate that the metal layer is deposited by a vapor deposition process, using in the exemplary embodiments, electroplating. **Schnur** does, however, indicate that the metal

deposition method is for use in interconnect for semiconductor microcircuitry (Abstract, Example 25 in col. 20.)

The basic textbook of **Wolf**, teaches that copper metal interconnect may be deposited by a variety of methods, including electroplating and vapor deposition methods such as PVD (e.g. sputtering) and CVD. (See pp. 782-783--especially p. 783, last paragraph before section 15.8.2.)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use a vapor deposition process, such as sputtering to deposit the metal layer in **Schnur**, because vapor deposition processes (i.e. PVD and CVD) are an art recognized equivalent means to the electroplating used in **Schnur** to form copper interconnect, as taught by **Wolf**.

Regarding claim 11, in Example 25 (col. 20) in **Schnur** the diffusion barrier coats the walls of a polysilicon steps, but it is unclear if the metal fills a hole in the substrate. But as noted above, **Schnur** states that the method is used for interconnect.

The basic textbook of **Wolf** teaches that copper interconnect fills a hole in a substrate lined with a barrier layer to form interconnect for semiconductor microcircuitry (Fig. 15-52, pp. 782-783).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form the metal interconnect of **Schnur** in a hole, because **Wolf** teaches that this is standard practice in the art to form copper interconnect.

Regarding claims 14 and 18, as noted above with respect to claim 7, Example 24 in **Schnur** states that the substrate is a silicon wafer with silicon oxide formed thereon.

Regarding claim 15, as noted above with respect to claim 8, **Schnur** discloses that the linear carbon chain of trichloro-(4-pyridyl)-ethyl-silane is the ethyl group, which has at least 2 carbon atoms.

Regarding claim 16, although **Schnur** does not teach sputtering, as noted above with respect to claim 9, **Wolf** teaches that PVD (of which sputtering is a member; Wolf, p. 438) is an art recognized means to electroplating to deposit metal films for interconnect.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use a vapor deposition process, such as sputtering to deposit the metal layer in **Schnur**, because vapor deposition processes (i.e. PVD and CVD) are an art recognized equivalent means to the electroplating used in **Schnur** to form copper interconnect, as taught by **Wolf**.

Regarding claims 17 and 19, it is held, absent evidence to the contrary, that the diffusion barrier of **Schnur** is capable of preventing the diffusion of metal atoms from the metal layer into the substrate when the semiconductor device is exposed to thermal annealing at 200 °C or an electric field of 2 MV/cm at 200 °C in flowing N_2 (claim 17) and that the semiconductor device does not exhibit $j_{leakage} > 1000\ nAcm^{-2}$ when the semiconductor device is exposed to thermal annealing at 200 °C or an electric field of 2 MV/cm in flowing N_2 at 200 °C for up to 650 minutes (claim 19). The basis for this reasoning is the same as applied to claim 10 above whose arguments are incorporated herein in their entirety. In short, equivalent structures must be capable of serving the same function. The structures in the instant specification are equivalent to those disclosed in **Schnur**.

Response to Arguments

7. Applicant's arguments with respect to all pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 703-306-5980. The examiner can normally be reached on 9:00 - 19:30 on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Erik Kielin
June 9, 2003